REMARKS

This paper is responsive to the Non-Final Office Action mailed on January 21, 2005. Claims 1-20 were examined and rejected. Applicants thank the Examiner for a detailed and thoughtful examination of all the claims.

Claims 1-8, 10-18, and 20 remain in this application. Claim 1, 11, and 17 are currently amended. Claims 9 and 19 are canceled.

Claim Rejections – 35 U.S.C. §112

Claims 1-20 stand rejected under 35 U.S.C. §112, first paragraph, as based on a disclosure which is not enabling.

Also, Claims 1-20 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding independent claims 1 and 11, Applicants have amended the claims to include the limitation of **a circuit for charging the first former-stage capacitor and the second former-stage capacitor**, which has been exemplified in the specification by the charging transistors N1 and N2 in FIGs. 3(a), 4(a), and/or 5. Such a limitation combined with the originally claimed limitations is believed to make independent claims 1 and 11 enabling as well as definite.

Regarding independent claim 17, Applicants have amended the claim to include the limitation of **charging the first former-stage capacitor and the second former-stage capacitor**, which has been exemplified in the specification by the charging transistors N1 and N2 in FIGs. 3(a), 4(a), or 5. Such a limitation combined with the originally claimed limitations is believed to make independent claim 17 enabling as well as definite.

Each of the claims dependent from claims 1, 11, or 17 is believed to be enabling and definite at least for this reason.

Claim Rejections – 35 U.S.C. §102(b)

Claims 1-20 stand rejected under 35 U.S.C. §102(b) as being anticipated by Tsai (USPAP 2002/0130703).

Regarding independent claim 1, Applicants have amended the claim to incorporate all of the limitations of the original claim 9, which is therefore canceled herein without prejudice or disclaimer. Such limitations, either in part or as a whole, are not disclosed or suggested by Tsai.

As pointed out by the Examiner, Tsai discloses, in Fig. 5, a clock Vphi2 provided to the capacitor in 108 and **exactly the same** clock Vphi2 also provided to the capacitor 132, which is a former-stage capacitor. However, the independent claim 1 (as amended) has limitations that:

> *a second clock falling edge of the second clock signal from the second clock high level to the second clock low level occurs earlier in time than a second former-stage clock falling edge of the second former-stage clock signal from the second former-stage clock high level to the second former-stage clock low level, and*
>
> *a second former-stage clock rising edge of the second former-stage clock signal from the second former-stage clock low level to the second former-stage clock high level occurs earlier in time than a second clock rising edge of the second clock signal from the second clock low level to the second clock high level,*

which have been exemplified in the specification by referring to FIGs. 4(b) or 6(b): a second clock (PCLK4) has **a narrower pulse width, completely covered in time within the same-phase pulse** of a second former-stage clock (PCLK2). Such a "the-latter-the-narrower" clock feature between former and latter stages further induce a reverse current prevention limitation:

> *thereby turning off the first switching circuit when the second clock signal and the second former-stage clock signal make transitions for preventing a first transition-state reverse current from flowing through the first switching circuit out of the first capacitor.*

Neither Tsai nor the prior art made of record in the Non-Final Office Action discloses or suggests this "the-latter-the-narrower" clock feature and the reverse current prevention limitation induced therefrom. Independent claim 1 is thus believed to be allowable over the art of record, and the claims dependent therefrom are likewise believed to be allowable at least for this reason.

As a point of clarity for the record, Applicants respectfully submit that the prior art "non-overlapping" clock feature actually refers to the two complementary clocks of the same stage (Vphi1 and Vphi2), and should not be confused with the Applicants' claimed "the-latter-the-narrower" clock feature between the former and latter stages.

Regarding independent claim 11, Applicants respectfully traverse the rejection

under 35 U.S.C. §102(b) as being anticipated by Tsai. As pointed out by the Examiner, Tsai discloses, in Fig. 5, a clock Vphi2 provided to the capacitor in 108 and **exactly the same** clock Vphi2 also provided to the capacitor 132, which is a former-stage capacitor. However, the independent claim 11 originally has limitations that:

> *a second clock falling edge of the second clock signal from the second clock high level to the second clock low level occurs earlier in time than a second former-stage clock falling edge of the second former-stage clock signal from the second former-stage clock high level to the second former-stage clock low level, and*
>
> *a second former-stage clock rising edge of the second former-stage clock signal from the second former-stage clock low level to the second former-stage clock high level occurs earlier in time than a second clock rising edge of the second clock signal from the second clock low level to the second clock high level,*

which have been exemplified in the specification by referring to FIGs. 4(b) or 6(b): a second clock (PCLK4) has **a narrower pulse width, completely covered in time within the same-phase pulse** of a second former-stage clock (PCLK2). Such a "the-latter-the-narrower" clock feature between former and latter stages further induce a reverse current prevention limitation:

> *thereby turning off the first switching circuit when the second clock signal and the second former-stage clock signal make transitions for preventing a first transition-state reverse current from flowing through the first switching circuit out of the first capacitor.*

Neither Tsai nor the prior art made of record in the Non-Final Office Action discloses or suggests this "the-latter-the-narrower" clock feature and the reverse current prevention limitation induced therefrom. Independent claim 11 is thus believed to be allowable over the art of record, and the claims dependent therefrom are likewise believed to be allowable at least for this reason.

Regarding independent claim 17, Applicants have amended the claim to incorporate all of the limitations of the original claim 19, which is therefore canceled herein without prejudice or disclaimer. Such limitations, either in part or as a whole, are not disclosed or suggested by Tsai.

As pointed out by the Examiner, Tsai discloses, in Fig. 5, a clock Vphi2 provided to the capacitor in 108 and **exactly the same** clock Vphi2 also provided to the capacitor 132, which is a former-stage capacitor. However, the independent claim 17 (as amended) has limitations that:

a second clock falling edge of the second clock signal from the second clock high level to the second clock low level occurs earlier in time than a second former-stage clock falling edge of the second former-stage clock signal from the second former-stage clock high level to the second former-stage clock low level, and

a second former-stage clock rising edge of the second former-stage clock signal from the second former-stage clock low level to the second former-stage clock high level occurs earlier in time than a second clock rising edge of the second clock signal from the second clock low level to the second clock high level.

which have been exemplified in the specification by referring to FIGs. 4(b) or 6(b): a second clock (PCLK4) has **a narrower pulse width, completely covered in time within the same-phase pulse** of a second former-stage clock (PCLK2).

Neither Tsai nor the prior art made of record in the Non-Final Office Action discloses or suggests this "the-latter-the-narrower" clock feature. Independent claim 17 is thus believed to be allowable over the art of record, and the claims dependent therefrom are likewise believed to be allowable at least for this reason.

Summary

In summary, claims 1-8, 10-18, and 20 are in the case. All of the claims are believed to be allowable over the art of record, and a Notice of Allowance to that effect is respectfully solicited.

Should any issues remain, Applicants respectfully requests a telephonic interview with the Examiner to discuss this response, and further in the hope that the remaining issues might be efficiently resolved.

Respectfully submitted,

Date: March 04, 2005

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Note: Please leave a message in my voice mail if you need to talk to me. The time in D.C. is 13 hours behind the Taiwan time, i.e. 9 AM in D.C. = 10 PM in Taiwan).